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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): **Marco Racanelli** Application Serial No.: **09/833,953** Filed: **April 11, 2001** Title: **Low Cost Fabrication of High Resistivity Resistors**	Group Art Unit: 2823 Examiner: Maldonado, Julio J.

REPLY BRIEF

Mail Stop Appeal Brief - Patents
Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This is a Reply Brief under 37 CFR § 41.41 in response to the Examiner's Answer dated April 11, 2006.

REMARKS

A. Response to Examiner's Answer

Applicant respectfully submits that each of independent claims 1 and 14 recite a series of steps that are performed in a specified sequence to advantageously achieve a low cost high resistivity resistor. It is the Examiner's position that the above limitations are disclosed in Zaccherini in view of Erdeljac and further in view of Shao. Applicant respectfully disagrees with the Examiner's characterization of Zaccherini, Erdeljac, and Shao, and with Examiner's interpretation of the above limitations.

1. Rejection of claims under 35 U.S.C. §103 over Zaccherini

In the Answer, the Examiner states:

> "Zaccherini (Fig. 1-6) teaches an analogous method to form semiconductor device including polysilicon resistors and transistors including forming a layer (7) comprising polycrystalline silicon over a transistor gate region (4) and a field oxide region (5) on a substrate (2,3); forming a doping barrier (10) above said polycrystalline silicon over said field oxide region (5) after forming said polycrystalline silicon layer (7); doping said layer over said transistor gate region with a first dose of a first dopant (11) after forming said doping barrier (10), wherein said first dose of said first dopant (11) is a dosage greater than required to result in said layer over said transistor gate region (4) having transistor gate electrical properties, wherein said first dopant (11) has a first conductivity type; removing said doping barrier (10 after doping said polycrystalline silicon layer (7) over said gate region (4) with said first dose of said first dopant (11); and doping said layer over said transistor gate region (4) and said field oxide region (5) with a second dose of a second dopant (13), after said step of removing said doping barrier (10) so as to form a high resistivity resistor in said layer (7) over said field oxide region (5), wherein said second dopant (13) has a second conductivity type, wherein said first dose of said first dopant is higher than said second dose of said second dopant, and wherein said

> resistor and said gate transistor region (4) are formed in a doped epitaxial layer (3), which is part of said substrate (2,3) (column 3, lines 1-53)." Answer, page 3, line 11 to page 4, line 7.

Applicant respectfully submits that both the method of manufacturing semiconductor devices and the structure disclosed in Zaccherini are sharply different than the method of manufacturing semiconductor devices and the structure found in the present invention. Therefore, the Examiner's conclusion is incorrect.

In contrast to the present invention as defined by independent claim 1, Zaccherini fails to teach, disclose, or suggest forming a layer over a transistor gate region, which is situated over a well in a substrate, and forming a layer over a field oxide region, which is situated in the substrate but not situated over the well, as specified in independent claim 1. In Zaccherini, polycrystalline layer 7 is formed over field oxide 5 and channel region 4, which are situated in epitaxial layer 3. Thus, since Zaccherini requires forming an additional layer (i.e. epitaxial layer 3) over substrate 2 prior to forming field oxide 5, channel region 4, and polycrystalline layer 7, the structure disclosed in Zaccherini is substantially different than the structure specified in independent claim 1. Also, Zaccherini does not teach, suggest, or provide any motivation for forming field oxide 5, channel region 4, and a well directly in substrate 2. Furthermore in Zaccherini, the respective implant dosage ranges of the N type dopant and the P type dopant overlap. In the Answer, the Examiner states:

> "Zaccherini dopes the same material with the same first and second dopant at doping dosages that overlap those claimed in the invention. Therefore since the same materials are treated the same way, the

same result would be obtained." Answer, page 9, lines 11-13.

Applicant respectfully disagrees that the materials are treated the same way and therefore the same result would be obtained. Zaccherini does not require the dosage of the N type dopant to be higher than the dosage of the P type dopant that is subsequently implanted in polycrystalline layer 7 across the entire wafer, as specified in independent claim 1. For example, in Zaccherini, a N type dopant can be implanted at an implant dosage of $5x10^{14}$ ions/cm^2 in polycrystalline layer 7 directly over channel region 4, and polycrystalline layer 7 can be subsequently doped across the entire wafer with a P type dopant at an implant dosage of $1x10^{15}$ ions/cm^2 after removal of photoresist 10, which protected the areas reserved for resistors 8. In this situation, the transistor gate electrical properties are affected by the second dose of the second dopant, unlike what is specified in independent claim 1. In Zaccherini, therefore, the materials are not treated the same way, which causes different results to be obtained than in the present invention.

2. Rejection of claims under 35 U.S.C. §103 over Zaccherini in view of Erdeljac

The Examiner argues that Zaccherini can be combined with Erdeljac to show that transistor regions can be formed in different areas of conductivity. Furthermore, the Examiner states:

> "It would have been within the scope of one of ordinary skill in the art to combine the teachings of Zaccherini and Erdeljac et al. to enable forming the gate transistors and field oxide regions of Zaccherini on the substrate of Erdeljac et al. because one of ordinary skill in the art at the time the invention was made would have been

> motivated to look to alternative suitable methods of forming the gate electrodes and the field oxide regions of Zaccherini and art recognized suitability for an intended purpose has been recognized to be motivation to combine." Answer, page 4, line 18 to page 5, line 3.

In contrast to the present invention as defined by independent claim 1, Erdeljac fails to teach, disclose, or remotely suggest a transistor gate region situated over a well and a field oxide region not situated over the well, where a high resistivity resistor is formed over the field oxide region and the field oxide region and the well are formed in a substrate, as specified in independent claim 1. In Erdeljac, gate 24 is formed in a first polysilicon layer situated over N well 18, which is formed in P- epitaxial layer 12, and resistors 32, 34, and 56 are formed in second polysilicon layer 28 on field oxide region 20, which is situated over P- epitaxial layer 12. Also, in Erdeljac, P- epitaxial layer 12 is formed on P+ substrate 10. Thus, since Erdeljac requires forming two polysilicon layers (i.e. first polysilicon layer situated over N well 18, and second polysilicon layer 28 on field oxide region 20), and also requires forming an additional layer (i.e. P- epitaxial layer 12), the structure disclosed in Erdeljac is substantially different than the structure as specified in independent claim 1. Also, Erdeljac does not teach, suggest, or provide any motivation for forming field oxide region 20, gate 24, and N well 18 directly in substrate 10.

Also, the fabrication method and resulting structure disclosed in Erdeljac is substantially different than the fabrication method and resulting structure disclosed in Zaccherini. For example, Zaccherini discloses forming a P doped resistor and a gate

terminal in the same polycrystalline layer (i.e., polycrystalline layer 7). In contrast, Erdeljac discloses a double-level polysilicon process that results in the formation of a gate (i.e., gate 24) in a first polysilicon layer and formation of resistor (i.e., resistors 32, 34, and 56) in a second polysilicon layer (i.e., second polysilicon layer 28). In **In re Gordon**, 733 F.2d 900, 902 (Fed. Cir. 1984), the Federal Circuit has set forth the obviousness determination (see also **In re Fitch**, 972 F.2d 1260 (Fed. Cir. 1992)):

> "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious *unless the prior art suggested the desirability of the modification*." (emphasis added).

Thus, for the above reasons, Appellant respectfully submits that the combination of Zaccherini and Erdeljac suggested by the Examiner is not based on any evidence of reason in the prior art that would have suggested to one of ordinary skill in the art the desirability of such modifications. Rather, the reason, suggestion and motivation for the modification proposed by the Examiner is impermissible hindsight reconstruction given the benefit of the Appellant's disclosure.

3. Rejection of claims under 35 U.S.C. §103 over Zaccherini in view of Erdeljac and further in view of Shao

The Examiner then argues that adding the teachings of Shao was to show the sequence of steps to form the contacts. Furthermore, the Examiner states:

> "It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Zaccherini and Erdeljac et al. with the teachings of Shao et al. to enable forming

> high doping areas and electrical contacts in the high resistivity resistor of Zaccherini and Erdeljac et al., as taught by Shao et al., since this would result in the formation of electrical points of contact." Answer, page 6, lines 10-14.

In contrast to the present invention as defined by independent claim 1, Shao fails to teach, disclose, or remotely suggest sequentially forming a silicide blocking layer over the field oxide region after doping the layer over the transistor gate region and the field oxide region with a second dose of the second dopant, then doping an outer portion of the layer over the field oxide region with a third dopant having the second conductivity type, and next, fabricating a contact region comprising a silicide over a high-doped region of the outer portion of the layer over the field oxide region, as specified in independent claim 1. In Shao, N+ implant 18 is performed into poly 2 layer 16 to form the conductivity level of NMOS gate 40 while masking the PMOS region of poly 2 layer 16. N+ implant 18 is also applied to the region in poly 2 layer 16 where load resistor 38 is to be formed so as to control the value that is established for the load resistor. Thus, since Shao requires performing N+ implant 18 in the regions of poly 2 layer 16 where NMOS gate 40 and load resistor 38 are to be formed, the structure disclosed in Shao is substantially different than the structure specified in independent claim 1. Also, Shao does not teach, suggest, or provide any motivation for forming a silicide blocking layer over the region in poly 2 layer 16 situated over field oxide region 12, then doping an outer portion of the region in poly 2 layer 16 situated over field oxide region 12 with a third dopant having the second conductivity type, and next, fabricating a contact region

comprising a silicide over a high-doped region of the outer portion of poly 2 layer 16 situated over field oxide region 12, as specified in independent claim 1.

As discussed above, independent claim 1 recites a series of steps that are performed in a specified sequence to advantageously achieve a low cost high resistivity resistor. However, the particular sequence of step specified in independent claim 1 is not disclosed, taught, or suggested in Zaccherini, Erdeljac, and Shao, either singly or in any combination thereof. Thus, Appellant respectfully submits that the combination of Zaccherini, Erdeljac, and Shao suggested by the Examiner does not and cannot result in the invention as defined by independent claim 1.

The fabrication method and resulting structure disclosed in Erdeljac is substantially different than the fabrication method and resulting structure disclosed in Zaccherini. Additionally, the fabrication method and resulting structure disclosed in Shao is substantially different than the fabrication method and resulting structure disclosed in either Erdeljac or Zaccherini. For the above reasons, Appellant respectfully submits that the combination of Zaccherini, Erdeljac, and Shao suggested by the Examiner is not based on any evidence of reason, suggestion, or motivation in the prior art that would have led one of ordinary skill in the art to make such modifications. Rather, the reason, suggestion and motivation for the modification proposed by the Examiner is impermissible hindsight reconstruction given the benefit of the Appellant's disclosure.

For the foregoing reasons, Appellant respectfully submits that the present invention, as defined by independent claim 1, is not suggested, disclosed, or taught by

Zaccherini, Erdeljac, and Shao, either singly or in any combination thereof. As such, the present invention, as defined by independent claim 1, is patentably distinguishable over Zaccherini, Erdeljac, and Shao. Moreover, claims 3-12 depending from independent claim 1 are, *a fortiori*, also patentably distinguishable over Zaccherini, Erdeljac, and Shao for at least the reasons presented above and also for additional limitations contained in each dependent claim.

Independent claim 14 recites similar limitations as independent claim 1 discussed above. Thus, for similar reasons as discussed above, Appellant respectfully submits that the present invention, as defined by independent claim 14, is not suggested, disclosed, or taught by Zaccherini, Erdeljac, and Shao. As such, the present invention, as defined by independent claim 14, is patentably distinguishable over Zaccherini, Erdeljac, and Shao. Thus, claims 15 and 17-23 depending from independent claim 14 are, *a fortiori*, also patentably distinguishable over Zaccherini, Erdeljac, and Shao for at least the reasons presented above and also for additional limitations contained in each dependent claim.

Accordingly, Appellant respectfully submits that independent claims 1 and 14, and their respective dependent claims, should be allowed.

B. Conclusion

Based on the foregoing reasons, the present invention, as defined by independent claims 1 and 14, and claims depending therefrom, is patentably distinguishable over the

art cited by the Examiner. Appellant respectfully requests a favorable decision on claims 1, 3-12, 14, 15, and 17-23 pending in the present application.

Respectfully Submitted,
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